(12) UK Patent Application (19) GB (11) 2 141 906 A

(21) Application No 8414624

(22) Date of filing 8 Jun 1984

(30) Priority data

(31) 8316719   (32) 20 Jun 1983   (33) GB

(71) Applicant
Independent Broadcasting Authority, (United Kingdom),
70 Brompton Road, London, SW3 1EY

(72) Inventor
John Lewis Edwin Baldwin

(74) Agent and/or address for service
A. A. Thornton & Co., Northumberland House, 303—306 High Holborn, London, WC1V 7LE

(51) INT CL³
H03K 13/24 G11B 5/09

(52) Domestic classification
H4P DCR
U1S 2104 H4P

(56) Documents cited
GB A 2083322   EP A2 0074656
GB A 2049371   EP A1 0071680
GB 1462889   EP A1 0059224
EP A1 0083407

(68) Field of search
H4C

(54) Recording of digital information

(57) Apparatus for recording digital information is organised on a word based arrangement and includes means for generating a code word (Fig. 1) for each input digital word to be recorded, the code word occupying the same time as the input digital word but having at least double the number of time slots with respect to the number of bit locations in an input digital word. In a code word, transitions, are not permitted in the first or last time slots and transitions must be spaced apart by a period equal to at least three time slots. Apparatus for generating the digital words from the codewords, for replaying the digital information recorded by the above apparatus is also disclosed.

FIG. I.

Fig.1.

Fig. 2.

8 BIT DATA WORD INPUT

WORD CLOCK

12

VC.OSC. 12a

÷18 12b

CO AMP 12c

CLOCK f SLOTS

CLOCK f WORDS

ADDRESS 10

ROM 256 × 16 BIT

DATA

LATCH 11
2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17

SERIALIZER 14
18 17 0 1 2 etc 0

÷2 15

LATCH 16

RECORD AMP 17

18

RECORD HEAD
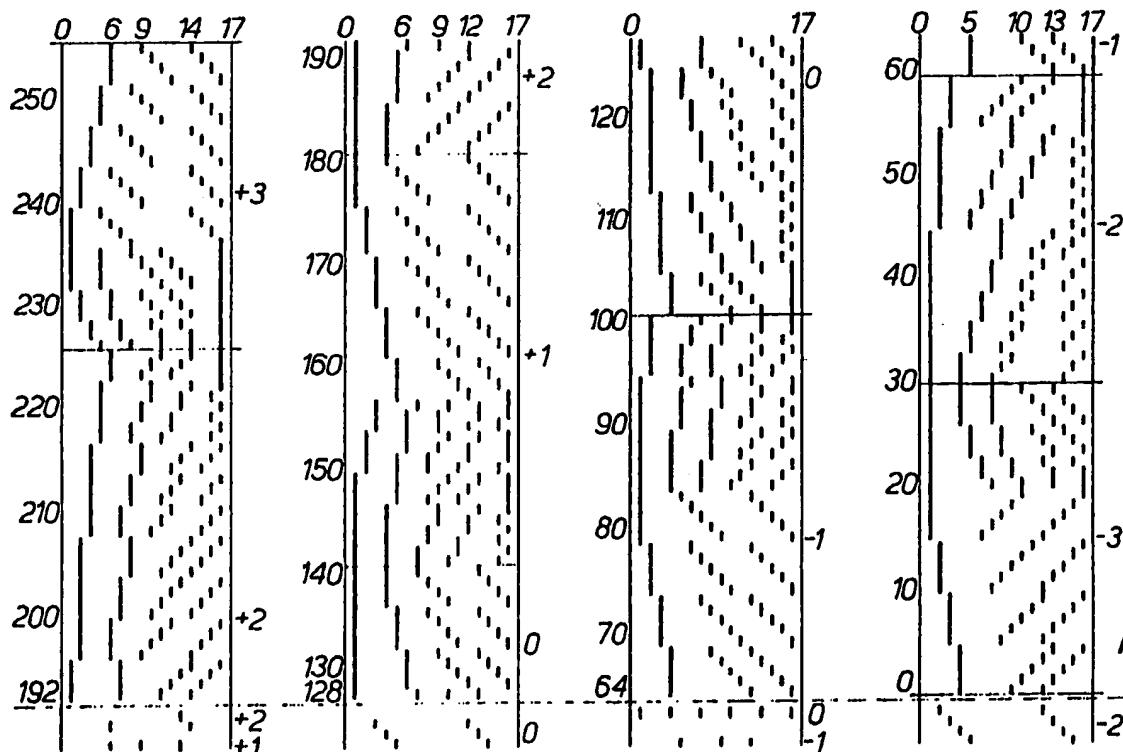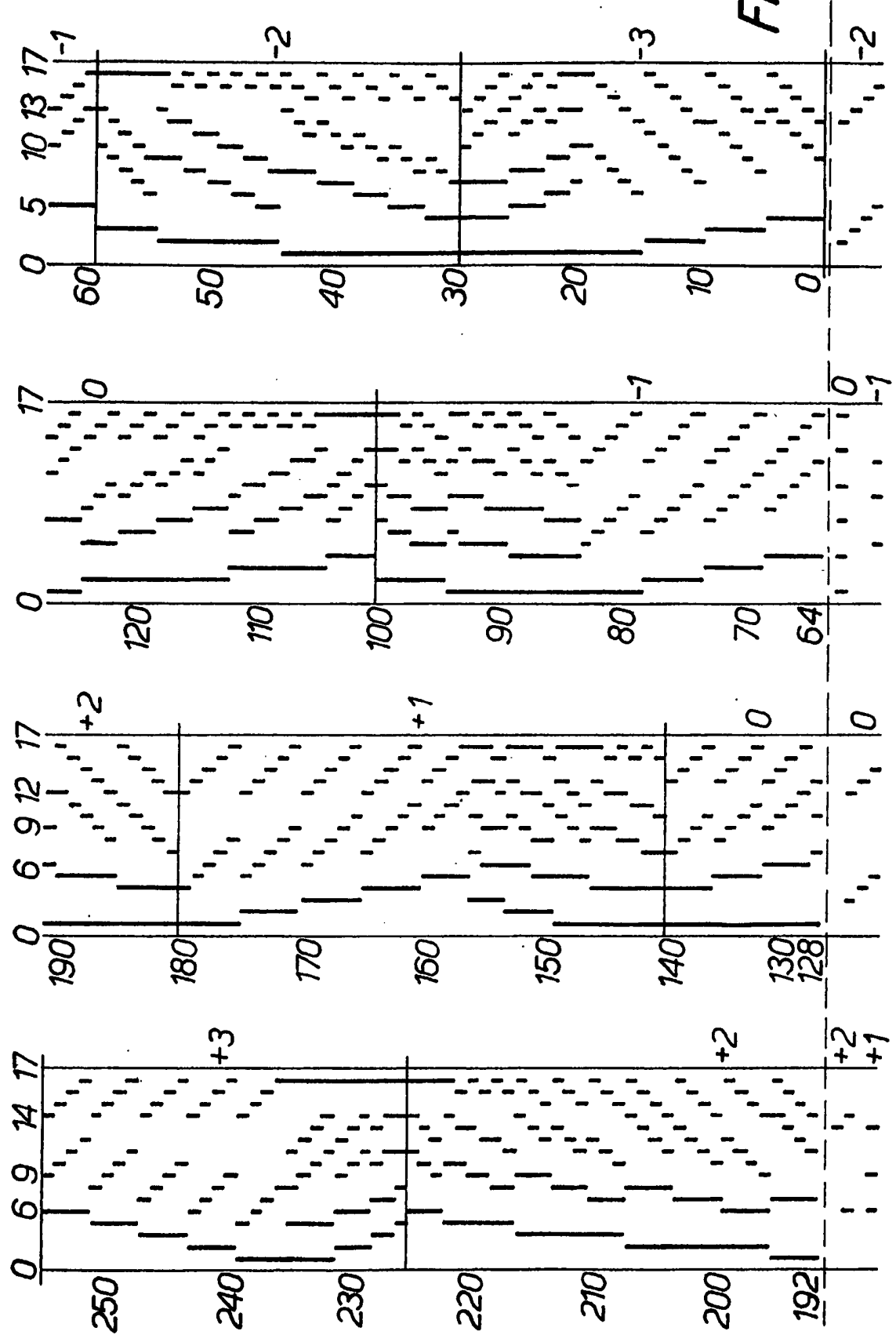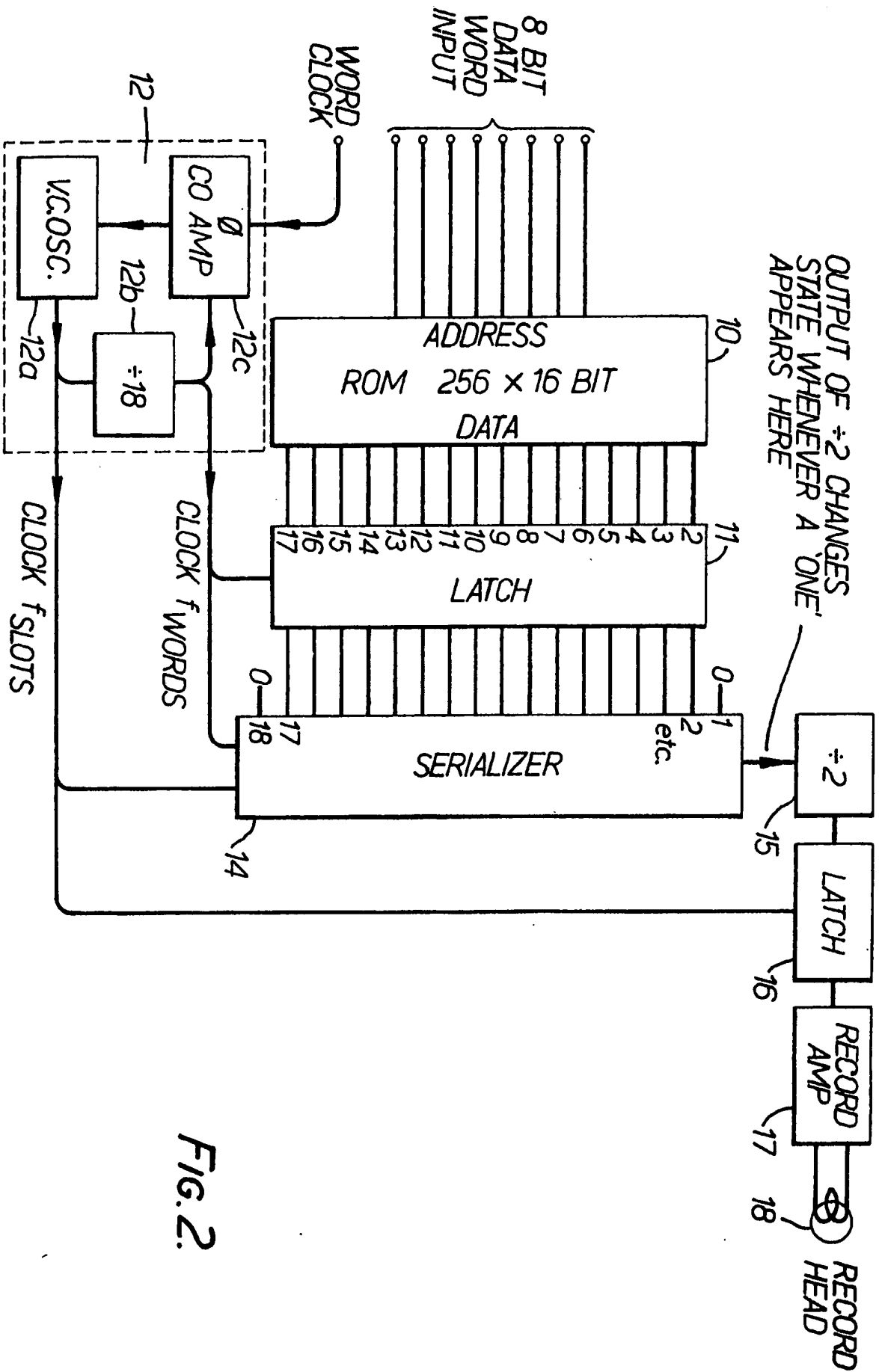
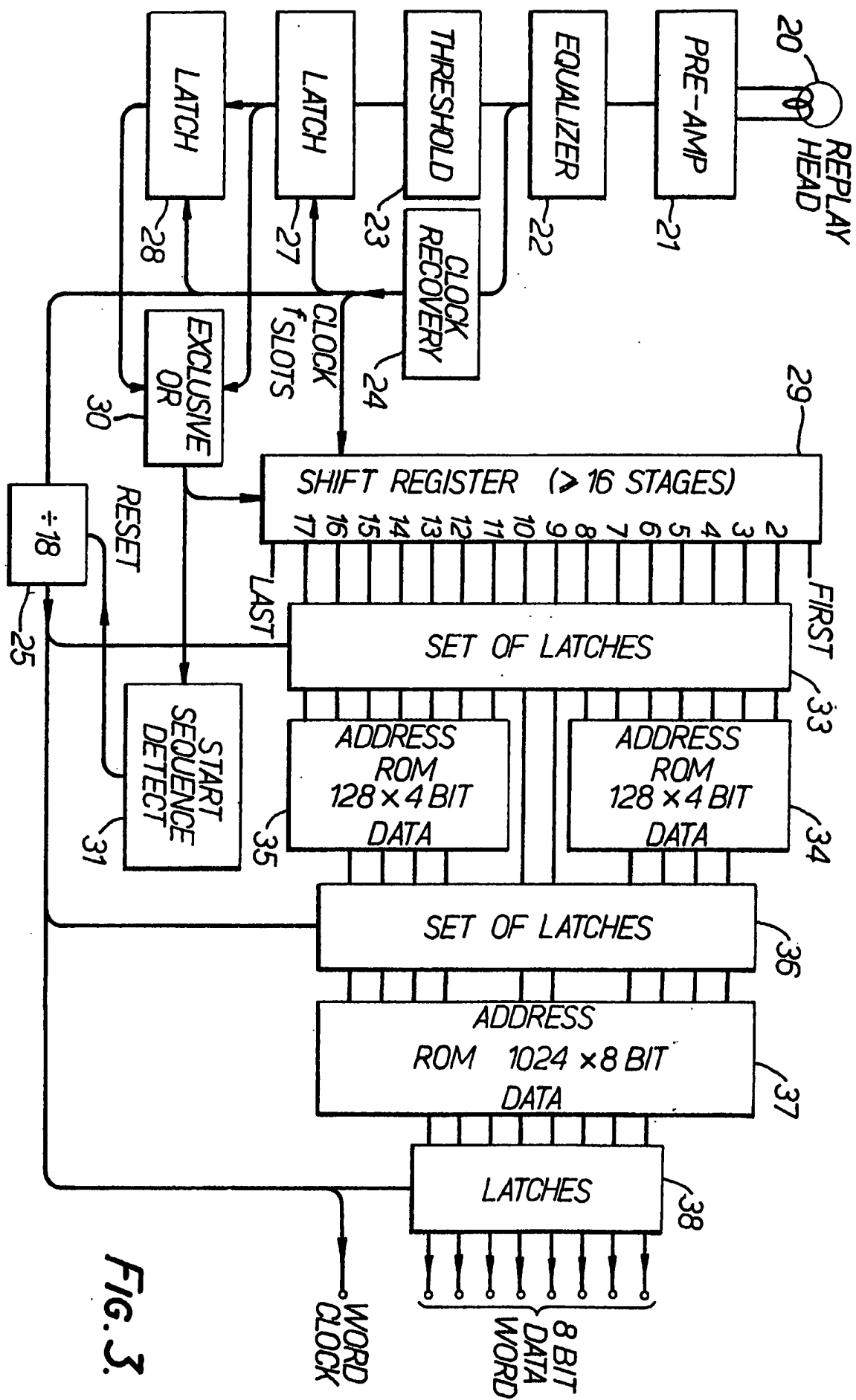OUTPUT OF ÷2 CHANGES STATE WHENEVER A 'ONE' APPEARS HERE

Fig. 3.

SPECIFICATION
Recording of Digital Information

The present invention relates to the recording
of digital information and more particularly but
5 not exclusively to the recording of television video
signals in digital form on magnetic tape.

For the purpose of the present specification we
will refer to the recording of video signals on
magnetic tape but it is to be understood that this
10 is but one specific embodiment; audio signals in
digital form may also be recorded and the
recording medium need not be magnetic tape.

In the tape recording of digitised video signals,
one of the important parameters is the
15 longitudinal packing density of the digital
information on the tape. Increases in packing
density are desirable and have been proposed
using Miller, Miller Squared or NRZ codes which
are bit organised systems.

20 It is an object of the present invention to
provide an arrangement which will allow an
increase in the minimum separation between
adjacent transitions compared to the previously
proposed systems.

25 The present invention provides an arrangement
based on a word organised system and includes a
code for encoding input data words and which
increases the number of bits in the encoded word
without increasing the time occupied by the code
30 word with reference to an input data word. The
number of bits in the encoded words or as they
will be referred to hereinafter, time slots, is $2n+a$
where n is the number of bits in the input data
word and a is an integer. Preferably, n is equal to
35 8 for video signals in which case a is in the range
of 2 to 8 inclusive and even more preferably in the
range of 2 to 5 inclusive.

Transitions are not permitted in the first or last
time slots of the encoded words but may occur in
40 any of the remaining time slots of a word
providing that the spacing between these
transitions satisfy other criteria as will be
explained later.

In order that the present invention be more
45 readily understood, an embodiment thereof will
now be described by way of example with
reference to the accompanying drawings, in
which:—

Figure 1 shows a preferred encoding
50 transformation for converting 256 levels into
encoded 18 bit words;

Figure 2 shows a block diagram of apparatus
for recording a signal using the transformation
shown in Figure 1; and

55 Figure 3 shows a block diagram of apparatus
for reproducing signals recorded using the
apparatus shown in Figure 2.

The basis of the preferred embodiment of the
present invention is a code, hereinafter called a
60 channel code.

It is possible to devise channel codes for the
magnetic recording of binary digital signals on
tape which perfectly provide certain desirable

characteristics e.g. a constant zero frequency
65 component.

The prime consideration for the channel code
to be described here is not the elimination of the
low frequency perturbations but to increase the
minimum separation between adjacent
70 transitions, compared to Miller, Miller Squared or
NRZ. This increase is in the ratio 4:3 in the
preferred embodiment; it might be reasonable to
conclude that this permits the longitudinal
packing density to be increased by $33\frac{1}{3}\%$.

75 The code is word based, the time of one word
being split into $2n+a$ equal units of time or time
slots. Transitions are not permitted in the first or
last of these but may occur in any of the
remaining providing these transitions are spaced
80 by at least three time slots; for example if a
transition is centred in time slot 6 then transitions
would not be permissible in 4, 5, 7, or 8. For the
purposes of this description, it is assumed that n
(the number of bits in an input data word) is 8 and
85 a is equal to 2 thus giving an 18 bit code word. Of
the total words available complying with these
constraints a first selection was made by rejecting
all words which had a direct component outside
of the range 41.66 to 58.34% for repeated words.

90 Further selection towards the desired range of
256 patterns of transitions, which number is
determined by the number of bits in an input data
word, was made by eliminating patterns in which
adjacent transitions were more than nine time
95 slots apart, patterns in which the first transition
was later than the sixth time slot or the last
transition was before the thirteenth time slot;
words with less than three transitions were also
eliminated.

100 This left 259 words. One of these patterns was
quite unique in that it contained six equispaced
transitions; two such words adjacent make a
pattern that cannot be duplicated by any
combination of other words even with incorrect
105 word framing. It seems appropriate to reserve this
word for the synchronising sequence; this leaves
258 patterns whereas 256 are required. Two
other patterns had first transitions at the sixth and
last transitions at the thirteenth time slot; this
110 makes them slightly less preferable than the
remaining words and hence these two were also
eliminated.

Above the dashed line in Figure 1 are shown
the 256 patterns of transitions selected for the
115 data whereas below the line are twelve of the
better patterns that have been rejected including
the special word containing six equispaced
transitions. These may be useful for synchronising
and control purposes. Above the dashed line are
120 four blocks each of 64 patterns of transitions and
the decimal numbering to the left of each block
indicates the suggested order. Words of similar
direct component are grouped together and
within this group, words with the same number of
125 transitions are also grouped.

If the signal were to start at plus 18 volts at the
beginning of the pattern and were to reverse sign
at each transition (giving a 36 volt peak-to-peak

signal) the figure to the right of each group gives the direct component (or average) in volts. For the words 226 to 255 inclusive this happens to be +3 voltages. However, if a word in this range
5 were followed by another from the same range the direct component cancels out. This results from there being an odd number of transitions so the second word will start at minus 18 volts. This is equally true for the three other ranges also
10 having an odd number of transitions and also of volts.

The three remaining ranges have an even number of transitions (and also of volts) and the cancellation of the direct component, should any
15 exist, will not occur.

If repeated, 181 of the 256 words will have a direct component of zero the remaining 75 words having a direct component differing by 5.55% of the peak-to-peak signal.

20 Run-length Statistics

	Separation of Adjacent Transitions (Time Slots)	Probability of Occurrence	
		Within Word	Between Words
	1	0	0
	2	0	0
	3	0.9375	0.1480
	—	—	—
30	8	0.0703	0.0726
	9	0.0312	0.0348
	10	0	0.0137
	11	0	0.0034
	12 or more	0	0

(margin notes: $d+1=3$; $K+1=11$; column labels at 25)

35 It can be seen that the ratio of the longest to the shortest transition spacing is 3:1; including the effects of the longer possible separations between transitions in adjacent words increases this ratio to 11:3.
40 The generation of these code words is not difficult; a solution based on a 256 address 16 bit ROM would be a straight-forward approach. The return from the channel code to the video data is more difficult, ROM with 65536 addresses of 8
45 bits seeming a little unreasonable. However, there are some subterfuges that can be used; for example; there are only 16 combination of permissible transitions in time slots 2 to 7 inclusive and also in time slots 10 to 17 inclusive.
50 Two read only memories each with 128 addresses of 4 bits can, therefore, reduce the combinations of transitions in 14 time slots into a total of 8 bits. These 8 bits together with 2 bits

representing transition information in time slots 8
55 and 9 can be decoded by a third ROM with 1024 addresses each of 8 bits. Many other practical decoding algorithms are possible; these include those based generally on the separation of adjacent transitions rather than the positions of
60 transitions.

For a better understanding of the generation of code words and how they may be recorded, attention is directed to Figure 2 which shows one form of recording apparatus for making use of the
65 code shown in Figure 1.

The basis of the recording apparatus is a memory device 10 in the form of a 256 address 16 bit ROM. Input data words each of 8-bits and each representing one of 256 levels are used to
70 address the memory device 10. Each 8-bit input data words generates a corresponding 16-bit output code word. Only 16 bits are required because the code has the constraint that no transitions may appear in the first or last time
75 slots. The output code word is retained in a latch 11 operated at word frequency by a clock signal from a clock circuit 12. The clock circuit 12 is based on a voltage controlled oscillator 12a running at, in this case, 18 times word frequency.
80 The output of the oscillator 12a is fed to a dividing circuit 12b which divides the oscillator output frequency by, in this case 18 to develop the word frequency clock signal. Synchronisation of the oscillator 12a, is ensured by feeding the
85 output of the dividing circuit 12b to a phase comparator circuit 12c where the word frequency from 12b is compared with a master word frequency clock signal to derive a control voltage for application to the oscillator 12a.
90 The 16-bit word in the latch 11 is clocked in parallel to a parallel to serial converter 14 whose first and last inputs are permanently connected to a logical 'O' signal whereby to produce the full 18-bit code word with no transitions in either the
95 first or last time slot. The serial output from the converter 14 is fed to a divide-by-2 circuit 15 whose output changes state whenever a logical 'one' signal appears at its input. The output of the circuit 15 is fed through a latch 16 to a record
100 amplifier 17 and thence to a recording head 18.

Figure 3 shows a part of playback apparatus for reproducing the signal recorded using the apparatus shown in Figure 2. The recorded signal is reproduced by the usual replay head 20 and the
105 signal fed via a pre-amp. circuit 21 and equalizer circuit 22 to a threshold circuit 23 and clock recovery circuit 24. Thus far, the circuit is conventional and will not be described in detail; suffice to say that the output of the clock recovery
110 circuit 24 is a signal whose frequency is the time slot frequency of the coded words. The output of the circuit 24 is fed to a dividing circuit 25 for producing a word frequency clock signal by dividing the output of the circuit 24 by $(2n+a)$
115 i.e. by eighteen. The output of the circuit 24 is also fed to two latches 27, 28 and shift register 29. The latches 27, 28 together with an EXCLUSIVE OR circuit 30 reconstitute the signal

(margin notes: $m,n = 8,16$)

to the form it took at the recording side prior to the divide-by-2 circuit 16 in Figure 2. In other words, a proper bit sequence is generated. This bit sequence which is the output from the
5 EXCLUSIVE OR circuit 30 is fed in serial form to a shift register 29 having at least 16 and preferably 18 stages. The bit sequence is also fed to a start detector circuit 31 which is used, among other things, to reset the word frequency producing
10 circuit 25 in detection of each start sequence.
  The output from the shift register 29 is fed in parallel to a 16-bit latch 33 whose output is a code word. This is decoded in the manner suggested above by feeding the seven bits of the
15 code word representing time slots 2 to 7 inclusive to a memory device 34 which transforms the seven bits into four bits and by feeding the seven bits of the code word representing time slots 10 to 17 inclusive to a memory device 35 which also
20 transforms the seven bits into four bits. The outputs of the memories 34 and 35 together with the bits representing time slots 8 and 9 are fed through a set of latches 36 to a third memory device 37 whose 8-bit output is one of the 8-bit
25 data words which had been recorded. This 8-bit word is fed to an output latch 38.
  From the above description, it will be seen that for a 12.5% increase of clock frequency compared to Miller or Miller Square, the channel code
30 described above enables a 33% increase in longitudinal packing density for the same minimum separation of transitions. There is a variation of the direct component of 8-bit words but this is never outside the range of
35 50%±8.33%; for repeated words, the limits are 50%±5.55% for unidirectional signals.
  Various modifications may be made, even to the code. For example the limitation that the transitions should be no closer than 3-time slots
40 could be increased but this would necessitate an increase in the number of time slots for a code word up to 24 bits for an 8-bit words.
  The code words are selected such that the direct component is well controlled within the
45 range 50%±15% the position within the range depending on the number of bits in the input word and the number of time slots in code word.

not selected between alternate code words for an info word

CLAIMS
  1. Apparatus for recording digital information
50 comprising means for receiving a succession of input digital words each comprising a plurality of bit locations, means for generating a respective code word for each digital word, with each code word having a number of time slots greater than
55 the number of bit locations in an input digital word with a minimum spring of a period equal to the period of three time slots between adjacent transitions, and means for recording the code words.
60   2. Apparatus according to claim 1, wherein the number of time slots in each code word is equal to (2n+a), where n is the number of bit locations and a is an integer ≥2.
  3. Apparatus according to claim 2, where n is
65 equal to 8 and a is in the range of 2 to 8 inclusive.
  4. Apparatus according to claim 3, where a is in the range 2 to 5 inclusive.
  5. Apparatus according to claim 4, where a is 2.   *8-18*
70   6. Apparatus according to any one of the preceding cliams, wherein said generating means includes a read only memory.
  7. Apparatus according to claim 6, wherein a parallel to series converter is provided operating
75 at (2n+a) times the input word frequency whereby each code word is converted into a serial stream prior to recording.
  8. Replay apparatus for recovering digital information recorded using apparatus according
80 to claim 1, and comprising replay head means for recovering the recorded code words each with a predetermined number of time slots in each word, means for receiving the recovered code words, means for regenerating digital words having
85 fewer bit locations than the number of time slots in a code word, and means for outputting the generated digital words.
  9. Apparatus according to claim 8, wherein the recorded signal is in the form of code words each
90 having (2n+a) time slots where n is equal to the number of bit locations in the original digital word to be recorded and a is an integer ≥2, and wherein the receiving means comprises at least 2n locations.
95   10. Apparatus according to claim 9, wherein the receiving means has (2n+a) locations.
  11. Apparatus according to claim 8, wherein the regenerating means comprises two memory devices each for regenerating a portion of a digital
100 word and latch means for assembling a regenerated digital word from the outputs of the two memory devices.
  12. Apparatus according to claim 11, wherein the latch means is arranged to receive output
105 directly from the receiving means in addition to the outputs from the two memory devices.